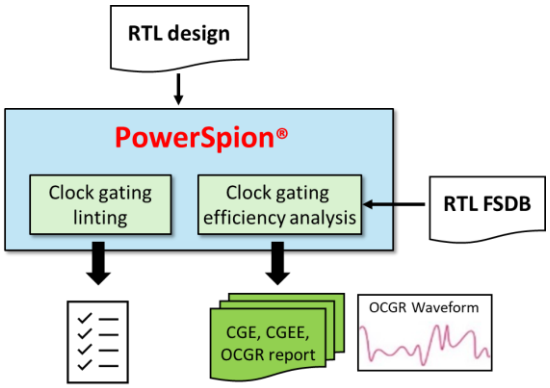
PowerSpion facilitates clock gating analysis and promotes low-power RTL development

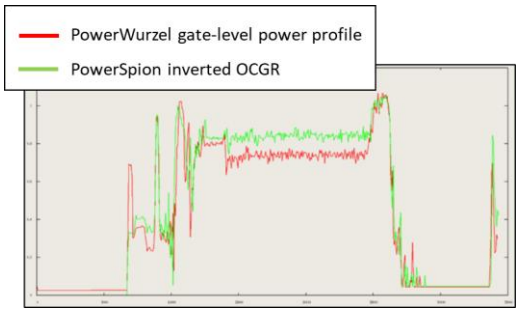
- Super fast and light
- Automatically extract inferred ICGs from RTL structure
- Clock gating metrics including OCGR waveform and report
- Static clock gating linting

PowerSpion extracts clock gating structure from RTL design and reports the effectiveness of clock gating by computing various clock gating metrics based on given FSDB or VCD files. This analysis does not involve running power estimation, which can be slow and resource-intensive, thereby providing a faster (upto 5x) and lighter analysis than other tools.
PowerSpion also offers clock gating linting feature that can help spot potential issues (e.g. redundant ICG, ungated memory or register) in an RTL design without requiring vector-based analysis. This feature enables early detection and correction of clock gating problems, facilitating more efficient and power-aware RTL development in early design cycle.



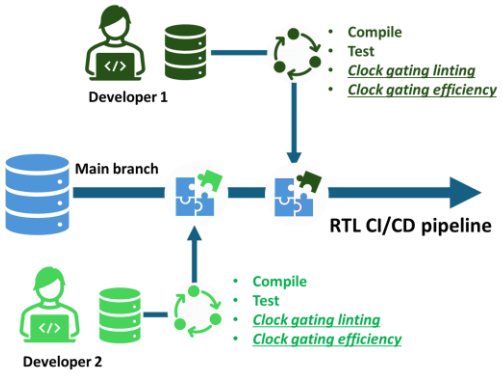
Clock Gating Efficiency Analysis and OCGR Waveform

PowerSpion provides essential clock gating efficiency metrics, such as CGE (clock gating efficiency), CGEE (clock gating enable efficiency), and OCGR (operational clock gating ratio). CGE is a useful metric for identifying areas to improve RTL for better clock gating, in addition to serving as an RTL sign-off criterion.
The OCGR waveform is particularly useful for those who want to monitor scenario-specific power waveform as it closely aligns with cycle-accurate power profiles. This metric is especially helpful when dynamic power constitutes a significant portion of the total power, such as in advanced technology nodes and data-intensive applications.



Power-aware RTL CI/CD Pipeline

RTL design team can promote low-power RTL development by seamlessly integrating PowerSpion into their RTL CI/CD pipeline. With PowerSpion integrated into the CI/CD pipeline, clock gating efficiency metrics and linting reports are recorded daily for the design team throughout the development cycle. This can help building a continuous and automatic understanding of low-power design techniques without extra effort from individual engineers.



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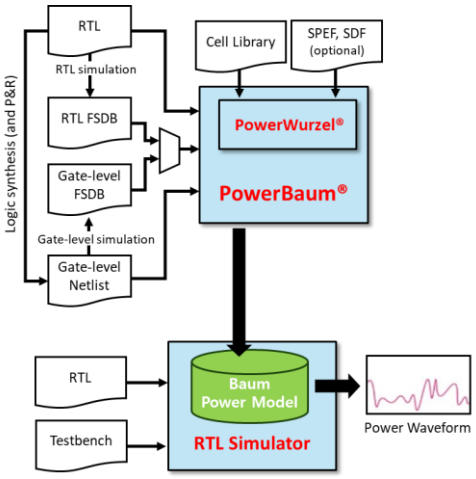
PowerBaum offers the fastest way to model and analyze power using realistic workload

- 100x faster than other solutions
- Parallel power modeling at any level of design hierarchy
- Supports multi-clock, multi-VDD and dynamic frequency scaling
- Power equation

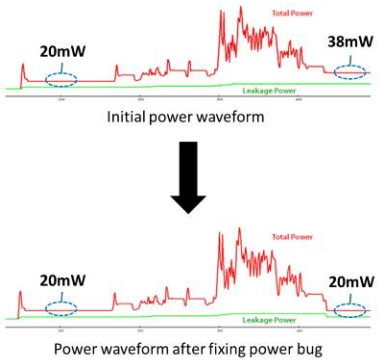
PowerBaum automatically generates fast and accurate power models that plug easily into a variety of third-party EDA tools such as HDL or ESL simulators. It enables system-level power analysis for an entire SoC with realistic workloads with billions of clock cycles.

PowerBaum takes RTL designs, cell libraries, gate-level netlists, and switching information (FSDB or VCD). It automatically generates a high-level power model of the given design in Baum's proprietary binary format. The power model is then linked with a commercial HDL or ESL simulator and generates power waveforms on-the-fly.
Early power-related design decisions have the most potential to minimize power consumption in a chip design. Integration of PowerBaum into RTL simulation is very easily making it very feasible for RTL optimization. RTL designers working on a variety of chip designs can use PowerBaum to analyze and minimize power consumption in the early design stage for the highest impact.



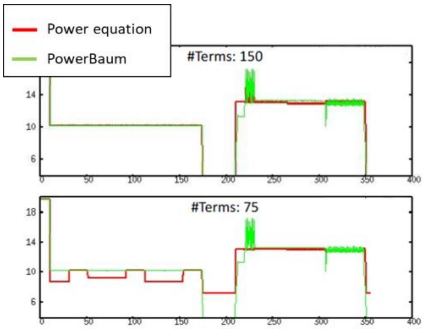
Power Debugging

Power debugging requires users to analyze billions of clock cycles running different scenarios to spot if there is any undesirable power consumption (i.e. power bug) lurking in the power profile.
PowerBaum allows users to run system-level simulation with realistic workloads and generate power profile which later can be analyzed for power debugging. With time-based power analysis capabilities provided in a form of power waveform, users can easily zero in on the exact parts of the design that are consuming excess power and fix it as illustrated in the figure.



Power Equation

With PowerBaum, user can automate the extraction of key signals from RTL designs and formulate a power equation. This equation includes 1st or 2nd order terms derived from the probability and switching activity of these signals. The resulting power equation can function as a rapid power analysis model or can be integrated into user's RTL design as on-chip power meter, facilitating real-time and fine-grained power management decisions such as Dynamic Voltage and Frequency Scaling (DVFS) to meet power and thermal budget or alleviate voltage drops.



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